

**WHAT IS CLAIMED IS:**

1           1.     A method of performing a fast information compare within a processor  
2 comprising:  
3           performing a more significant bit compare when information is loaded into a  
4           translation lookaside buffer, the more significant bit compare  
5           comparing more significant bits of the information being loaded into  
6           the translation lookaside buffer with more significant bits of compare  
7           information;  
8           storing a result of the more significant bit compare within the translation  
9           lookaside buffer as part of an entry containing the information;  
10          using the result of the more significant bit compare in conjunction with results  
11          from a compare of less significant bits of the information and less  
12          significant bits of compare information to determine whether a match  
13          is present.

1           2.     The method of claim 1 further comprising:  
2 providing an indication of a match to the compare information when the result  
3           of the more significant bit compare is active and the less significant  
4           bits of the information match the less significant bits of the compare  
5           information.

1           3.     The method of claim 1 wherein:  
2 the compare information corresponds to a virtual address watchpoint; and  
3 the result of the more significant bit compare indicates that the more  
4           significant bits of the information being loaded correspond to more  
5           significant bits of a watchpoint address.

1           4.     The method of claim 1 wherein:  
2 the compare information corresponds to sample selection criteria; and  
3 the result of the more significant bit compare indicates that the more  
4           significant bits of the information being loaded correspond to the  
5           sample selection criteria.

1        5.     The method of claim 4 wherein:  
 2        the sample selection criteria includes a sample selection criteria low address, a  
 3                sample selection criteria high address and sample selection criteria mid  
 4                address; and  
 5        the result of the more significant bit compare indicates whether the more  
 6                significant bits of the information being loaded correspond one of a  
 7                plurality of conditions indicated by the sample selection criteria.

1        6.     The method of claim 1 wherein:  
 2        the processor includes a memory management unit translation lookaside buffer  
 3                and an instruction translation lookaside buffer; and  
 4        the more significant bit compare is performed when information is loaded into  
 5                the instruction translation lookaside buffer.

1        7.     The method of claim 1 wherein:  
 2        the processor includes a plurality of threads; and  
 3        the compare information is unique for each of the plurality of threads.

1        8.     An apparatus for performing a fast information compare within a  
 2 processor comprising:  
 3        means for performing a more significant bit compare when information is  
 4                loaded into a translation lookaside buffer, the more significant bit  
 5                compare comparing more significant bits of the information being  
 6                loaded into the translation lookaside buffer with more significant bits  
 7                of compare information;  
 8        means for storing a result of the more significant bit compare within the  
 9                translation lookaside buffer as part of an entry containing the  
 10                information;  
 11        means for using the result of the more significant bit compare in conjunction  
 12                with results from a compare of less significant bits of the information  
 13                and less significant bits of compare information to determine whether a  
 14                match is present.

1        9.     The apparatus of claim 8 further comprising:  
 2        means for providing an indication of a match to the compare information when  
 3                the result of the more significant bit compare is active and the less  
 4                significant bits of the information match the less significant bits of the  
 5                compare information.

1        10.    The apparatus of claim 8 wherein:  
 2        the compare information corresponds to a virtual address watchpoint; and  
 3        the result of the more significant bit compare indicates that the more  
 4                significant bits of the information being loaded correspond to more  
 5                significant bits of a watchpoint address.

1        11.    The apparatus of claim 8 wherein:  
 2        the compare information corresponds to sample selection criteria; and  
 3        the result of the more significant bit compare indicates that the more  
 4                significant bits of the information being loaded correspond to the  
 5                sample selection criteria.

1        12.    The apparatus of claim 11 wherein:  
 2        the sample selection criteria includes a sample selection criteria low address, a  
 3                sample selection criteria high address and sample selection criteria mid  
 4                address; and  
 5        the result of the more significant bit compare indicates whether the more  
 6                significant bits of the information being loaded correspond one of a  
 7                plurality of conditions indicated by the sample selection criteria.

1        13.    The apparatus of claim 8 wherein:  
 2        the processor includes a memory management unit translation lookaside buffer  
 3                and an instruction translation lookaside buffer; and  
 4        the more significant bit compare is performed when information is loaded into  
 5                the instruction translation lookaside buffer.

1       14.    The apparatus of claim 8 wherein:  
2       the processor includes a plurality of threads; and  
3       the compare information is unique for each of the plurality of threads.

1       15.    A processor comprising:  
2       a translation lookaside buffer; and  
3       a first compare unit coupled to the translation lookaside buffer, the first  
4             compare unit performing a more significant bit compare when  
5             information is loaded into a translation lookaside buffer, the more  
6             significant bit compare comparing more significant bits of the  
7             information being loaded into the translation lookaside buffer with  
8             more significant bits of compare information, the first compare unit  
9             storing a result of the more significant bit compare within the  
10            translation lookaside buffer as part of an entry containing the  
11            information;  
12       a second compare unit coupled to the translation lookaside buffer, the second  
13            compare unit processor using the result of the more significant bit  
14            compare in conjunction with results from a compare of less significant  
15            bits of the information and less significant bits of compare information  
16            to determine whether a match is present.

1       16.    The processor of claim 15 wherein:  
2       the second compare unit provides an indication of a match to the compare  
3             information when the result of the more significant bit compare is  
4             active and the less significant bits of the information match the less  
5             significant bits of the compare information.

1       17.    The processor of claim 15 wherein:  
2       the compare information corresponds to a virtual address watchpoint; and  
3       the result of the more significant bit compare indicates that the more  
4             significant bits of the information being loaded correspond to more  
5             significant bits of a watchpoint address.

1       18.    The processor of claim 15 wherein:  
2       the compare information corresponds to sample selection criteria; and  
3       the result of the more significant bit compare indicates that the more  
4             significant bits of the information being loaded correspond to the  
5             sample selection criteria.

1       19.    The processor of claim 18 wherein:  
2       the sample selection criteria includes a sample selection criteria low address, a  
3             sample selection criteria high address and sample selection criteria mid  
4             address; and  
5       the result of the more significant bit compare indicates whether the more  
6             significant bits of the information being loaded correspond one of a  
7             plurality of conditions indicated by the sample selection criteria.

1       20.    The processor further comprising:  
2       a memory management unit, the memory management unit including a  
3             memory management unit translation lookaside buffer; and  
4       an instruction fetch unit, the instruction fetch unit including an instruction  
5             translation lookaside buffer, the more significant bit compare being  
6             performed when information is loaded into the instruction translation  
7             lookaside buffer.

1       21.    The processor of claim 15 wherein:  
2       the processor includes a plurality of threads; and  
3       the compare information is unique for each of the plurality of threads.